



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)	Group Art Unit: 2814
Hideomi SUZAWA et al.)	Examiner: D. Wille
Serial No. 10/086,628)	CERTIFICATE OF MAILING I hereby certify that this correspondence is
Filed: March 4, 2002)	being deposited with the United States Postal Service with sufficient postage as First Class
For: SEMICONDUCTOR DEVICE AND)	Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450,
MANUFACTURING METHOD)	Alexandria, VA 22313-1450, on June 30, 2005.
THEREOF)	addem Stamper

AFTER FINAL RESPONSE

Honorable Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

The Official Action mailed March 30, 2005 has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on January 8, 2004; January 22, 2004; and March 10, 2004.

Paragraph 2 of the Official Action rejects claims 8, 9, 19, and 20 as obvious based on the combination of Na et al., Ono et al., and Williams et al. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the



prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In accordance with the present invention two etching steps are performed: (1) a first etching step as shown in Figure 2C, for example; and (2) a second etching step shown in Figure 4A, for example. Claim 8, for example, recites "etching the metal film, the second amorphous semiconductor film and the first amorphous semiconductor film continuously to form a side edge of the first amorphous semiconductor film into a taper shape;" and subsequently recites "etching the transparent conductive film, the metal film, the second amorphous semiconductor film and the first amorphous semiconductor film to expose a part of the first amorphous semiconductor film, to form a pixel electrode from the transparent conductive film, to form a source wiring from the metal film and to form a source region and a drain region from the second amorphous semiconductor film."

With respect to all of the independent claims, it appears the Official Action may be relying on "metal layer 471" to teach the "metal film" of the independent claims of the present invention. If this is the case, then the Official Action appears to be asserting that Na teaches etching the metal film (conductive layer 471), the second amorphous semiconductor film (highly doped amorphous silicon layer 44) and the first amorphous semiconductor film (amorphous silicon layer 16) continuously to form a side edge of the

first amorphous semiconductor film (Figure 5F; column 4, lines 61-65). However, if this is the case, the patterning step shown in Figure 5F and column 4, lines 61-65 cannot also be relied upon to teach the second etching step of the claims of the present invention, i.e. "etching the transparent conductive film, the metal film, the second amorphous semiconductor film and the first amorphous semiconductor film to expose a part of the first amorphous semiconductor film, to form a pixel electrode from the transparent conductive film, to form a source wiring from the metal film and to form a source region and a drain region from the second amorphous semiconductor film." That is, Na does not appear to teach a first etching step wherein a metal film is etched, and a second etching step as in the present invention.

Thus, Na fails to disclose the first, continuous etching step, including etching of the metal layer, of the subject invention since Figure 5D of Na fails to disclose etching of a metal layer. Furthermore, if the Official Action is relying on Figure 5F of Na to show etching of the metal layer, than Na fails to disclose any etching corresponding to the claimed second etching step of the subject invention. Since Na fails to disclose or suggest each and every limitation of the claims, taken alone or in combination with Ono or Williams, a prima facie case of obviousness cannot be maintained and favorable reconsideration is requested.

Further the statement in the last 4 lines on page 2 of the Official Action appears to misunderstand the present invention with respect to the etching of the metal film. That is, this portion of the Official Action appears to assert that the etching of Na would inherently use the same gas since there is no distinction between the Si layers in Na. However, since a metal film is distinct from an Si film, Na would not necessarily (i.e. inherently) perform a continuous etching process (or etching without changing the etching gas).

With respect to independent claims 8, 9, 19 and 20, Na and Ono further do not teach or suggest etching a first amorphous semiconductor film (see Na, Figure 5F,

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reference 16; and Ono, Figure 16, reference AS) when forming a pixel electrode, a source wiring, a source region and a drain region.

Finally, the alleged motivation for combining Na and Ono (to provide a tapered portion to prevent breakage and form a more reliable device) can be achieved from the device of Ono alone and thus there is no need to combine the device of Ono with Na. Rather, since Na fails to recognize this as a problem, one of skill in the art would merely be led to practice Ono alone in view of the asserted motivation.

For all of the above reasons, it is respectfully submitted that a prima facie case of obviousness cannot be maintained. Reconsideration is requested.

Paragraph 4 of the Official Action rejects claims 10-12, 16-18, 21-26, and 28 as obvious based on the combination of Na et al., Ono et al., and Williams et al. Paragraph 6 of the Official Action rejects claims 13-15 and 27 as obvious based on the combination of Na et al., Ono et al., and Williams et al. These rejections, however, fail to overcome the deficiencies noted above and these claims are believed to be allowable for the same reasons as discussed above.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson

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